

Remarks

Claims 1-33 are pending and all claims are rejected. Claims 1, 7, and 33 are independent claims. Claims 1, 7, 15, 16, 18, 19 and 33 are amended herein.

The Specification was amended to correct a minor typographical error in the description of FIG. 5. In particular, (a reference to subsystem 210a was changed so as to refer to subsystem 120a, as supported by FIG. 5 as filed. No new matter was added. The reference to "210a" in the original text is an inadvertent error, as element 210a is not shown in FIG. 5, although in FIG. 5 a listed element 210 refers to a power source that is part of the Common Power Source 110.

Rejections Under 35 USC 112 and counter-response to Examiner's Response to Applicants' Arguments

Claims 1-33 are rejected under 35 USC 112 as failing to comply with the written description requirement on two grounds: (a) first (regarding claims 1, 7, 15, 19, and 33) that the Specification as filed does not teach certain limitations of claims 1, 7, 15, 19 and 33, namely that the Specification as filed "does not teach said mathematical equation which determines the interconnections" (namely, $K*((k-1)/2)$)" and that the amendment to the specification dated 8/4/2006 was "inappropriate" and allegedly added new matter (this allegation was made in the "Response to Arguments" section of the Office Action) ; and (b) second, that the equation $(k(k-1)/2)$ allegedly "does not provide the correct number of interconnections". Applicants respectfully disagree with (a) and (b), as the below explanation shows. Applicants also want to clarify the meaning of "interconnection" as it is intended in the claims and specification, in contrast with how the Examiner apparently is interpreting this term. Applicants also explain why their amendment to the specification that corrected the given equation so that it properly referenced this equation is not new matter, but rather restatement of something inherent in the Figures as filed (by virtue of the equation itself being known in the art).

First, Applicants maintain that the equation $(K * ((k-1)/2))$ is a straightforward simplification of the well-known classic algebraic formula for finding the number of possible

combinations M of objects selected from a set of n distinct objects taken r at a time, where, for the conditions of FIG. 2, as filed, Applicants have simplified this for the case where $r = 2$ (i.e., an **interconnection that connects just two components**, as is true for the instant claims and FIG. 2, as filed). To assist in the Examiner's understanding, Applicants have located a listing of this well-known formula in the classic mathematical reference: Samuel M. Selby, ed. CRC Standard Mathematical Tables (14th Ed., 1964) at page 392 (a copy of which is attached hereto as Exhibit A). This algebraic formula states, for finding the number of possible combinations M of objects selected from a set of n distinct objects taken r at a time:

$$M = \frac{n!}{r!(n-r)!}$$

For the case where $r = 2$:

$$M = \frac{n!}{2(n-2)!}$$

Now, it is, of course, known that:

$$n! = n * (n-1) * (n-2) * (n-3) * (etc...)$$

therefore:

$$(n-2)! = (n-2) * (n-3) * (n-4) * (etc)!$$

and it follows that:

$$n! = n * (n-1) * (n-2)!$$

This further simplifies the above M equation to be:

$$M = \left(\frac{1}{2}\right) \frac{n * (n-1) * ((n-2)!)}{(n-2)!}$$

Divide top and bottom by $(n-2)!$ results in:

$$M = \left(\frac{1}{2}\right) \frac{n * (n-1)}{1}$$

which is equivalent to:

$$M = (n) * \frac{(n-1)}{2}$$

In Applicants' Specification as filed, slightly different variable names were used, but it was clearly stated that the total number of subsystems = $m * n$ (where, as is apparent from FIG. 2, m is the number of rows and n is the number of columns). Because, as FIG. 2 shows, m and n are, inherently, both real, nonzero, positive integers, their product $m * n$ necessarily is a real, positive, nonzero integer, as well. For convenience and simplicity of expression, Applicants hoped by amendment to replace repeated use of the product $m * n$ with a single real, positive integer k . Applicants do not believe such a substitution is new matter, and Applicants' arguments are accurate regardless of whether or not $m * n$ or k is used.

Thus, per the algebraic equations above, for k (or $m * n$) subsystems, the number of combinations of any 2 of them (i.e., interconnections between any two of them) necessarily and inherently must be $k * ((k-1)/2)$ (or, if Examiner prefers, $(m * n) * (((m * n) - 1)/2)$) because of the aforementioned classic and well-known algebraic formula). In the application as filed, a typographical error resulted in this formula being listed incorrectly as $m * n - 1$ (i.e., $k - 1$) instead of as $(m * n) * ((m * n) - 1)/2$ (which would be $k * (k - 1)/2$). This error would be readily recognized by and obvious to one of skill in the art after viewing FIG. 2 and assuming knowledge of the basic algebraic formula given above. Furthermore, the formula as originally intended clearly is supported by the Figures as originally filed as being straightforward algebra long known in the art, and most certainly NOT new matter.

Applicants also now address the Examiner's assertion that the assertions that the above formula allegedly "does not provide the correct number of interconnections," because "each line between subsystems 120 in Figure 2 represents multiple power and signal connections between the subsystems 120." It appears that the Examiner is confused about what Applicants mean by "interconnection" in the claims as compared with what is meant by the Specification's reference to "multiple power and signal connections" or "conductors". Claim 1, as amended herein, refers to a plurality of *independent direct interconnections between the respective one of the k load subsystems and each other one of the k load subsystems*, where each *independent direct*

interconnection connects a given load subsystem to just one other given load subsystem. Applicants' acknowledge that each independent direct interconnection can itself comprise one or more conductors, but they are all part of the same interconnection. This is supported by the Application and Figures as filed. For example, see page 4, lines 14-17 of the Specification as filed, which explains that, in FIG. 2, each line (i.e., interconnection) between a subsystem and the common power source, or between subsystems, represents to "multiple power and signal connections"; see also page 7, line 18, stating that "power flows through multiple conductors"; and page 7, line 21 through page 8, lines 17, which refer to signals carried by individual conductors of a the system interconnect, e.g., page 8, lines 6-7, which state "Power from power source 116a also flows from subsystem 210a to subsystem 120b through conductor 3, 4 and 6 of the system interconnect" (noting that the "system interconnect" is the interconnect between subsystem 210a and subsystem 120b.)

What is important to understand is that, as used in the Specification, Claims, and Figures of the instant application, a given **interconnect** between two elements, which itself may contain one or more conductors, is still considered to be a single electrical interconnection between the two elements. The multiple power and signal connections (or multiple conductors) referred to in the Specification and Figures as filed are all part of the same single independent direct electrical interconnection, as claim 1, as amended indicates. One of skill in the art of power systems (the field of the invention) readily recognizes that such an interconnect between power systems typically is made using a cable, especially a multi-wire/multi-strand cable (i.e., multiple conductors), including signal line, ground line, return line, etc., as is well-understood in the art of electrical power system design. In the art, such an interconnection that itself includes multiple conductors is, for simplicity, commonly drawn as a single interconnect line (versus showing each individual conductor), although illustrating the individual conductors of the single interconnect line is sometimes applicable, as shown in FIG. 6 of the instant application.

As an example of the art, consider the bulk power voltage buses 102, 104 shown in FIGs. 1, 2, and 3 of US 5422561 to Williams (a reference cited herein), which buses are illustrated in these Figures of Williams via a single line, yet it is known in the art that bulk power buses for

power transmission inherently will include multiple conductors. For example, Williams explains that these voltages can be transformed down to a *three phase* secondary voltage (col. 1, lines 40-50), on a secondary bus 106 (Williams at col. 6, lines 19-43), where the secondary bus 106 is illustrated in FIG. 3 of Williams via a single line, yet those of skill in the art are well aware that three phase power necessarily requires three separate conductors, even if the three phase connection itself is shown as a single electrical connection. Accordingly, Applicants maintain that their illustration in FIG. 2 of an interconnect between subsystems, where the interconnect itself can comprises one or more conductor and signal lines, is consistent with use in the art and does not intend or imply that there are multiple independent interconnects between subsystems.

In addition, consider, for example, FIG. 2 of Applicants' application, and more particularly consider common power source 110, the subsystem 120 labeled as (1,1) (i.e., row 1, column 1) and the subsystem 120 labeled (1, j) (i.e., row 1, column j). Between the subsystem 120 (1,1) and common power source 110 there is but one interconnect, which for this example can be considered a first interconnect. Between the subsystem 120 (1,j) and common power source 110 there also is but one interconnect, which for this example can be considered a second interconnect, and it is seen clearly that this second interconnect is separate and distinct from the first interconnect. Similarly, between the subsystem 120 (1,1) and the subsystem 120 (1,j) there also is but one interconnect, which can be considered a third interconnect, which third interconnect is separate and distinct from the aforementioned first and second interconnects. Each of the first, second, and third interconnects respectively can comprise "multiple power and signal connections", where the multiple power and signal connections are respective conductors that are part of the respective interconnect and cooperate to connect together electrically only that which is already connected together in the interconnect itself. There are NOT "multiple interconnections" between subsystems, but there can be multiple conductors that are part of a single given interconnect (which interconnect itself may or may not include multiple conductors).

The Examiner refers to FIG. 5 in an attempt to show that the claimed formula for the number of interconnects between power subsystems and between power subsystems and the

common power source does not satisfy the formula of $[k*(k-1)/2]$ recited in the claims. For example, the Examiner asserts that the connections labeled 3, 4, 5, and 6 of FIG. 5 are “interconnects”. This is incorrect. As Applicants explained thoroughly above, and in the Specification as filed, these connections are conductors that are themselves part of an interconnect. For example, Applicants refer to page 7, line 10 through page 8, line 17, of Applicants’ Specification, which states clearly that these connections labeled 3, 4, 5 and 6 of the FIG. 5 are **conductors**, not interconnections (e.g., in FIG. 5, conductors 3, 4, and 6 of the “system interconnect” between subsystem 120a and 120b).

Thus, it also should be clear that, in connection with claim 1, a given first direct independent interconnect can itself comprise one or more conductors, such as individual conducting wires, e.g., signal, return, and ground, all of which cooperate together to form the first direct independent interconnect. A second interconnect may exist that connects (using one or more conductors, such as wires or other conductors) a different pairing of components than does the first interconnect.

The rejections under 35 USC 112 also included some concern/rejections regarding terminology and antecedent basis issues, and Applicants believe that the amendments in this response address those concerns, by either correcting or eliminating the language at issue

For example, in claim 1 the language “the plurality of power subsystem components comprising k subsystem components,” which was deemed unclear, has been removed and replaced with consistent reference to “k load subsystems.” The phrases “the plurality of power subsystem components” and “the plurality of interconnection” lines (each of which was deemed to lack antecedent basis) have been deleted and replaced with other language.

Rejections Under 35 USC 102.

The Examiner rejected Claim 33 under 35 U.S.C. §102 as being anticipated by Williams et al. Claim 33, as amended herein, recites [emphasis added]:

A power system comprising:

at least one common power source component;

k power subsystem components, each respective one of the k power subsystem components having a corresponding direct, independent first electrical interconnection that originates at the common power source component and terminates at the respective one of the k power subsystem components without coupling to any other of the k load subsystems;

for each respective one of the k power subsystem components, a plurality of direct independent second electrical interconnections between the respective one of the k power subsystem components and each other one of the k power subsystem components, each direct independent second electrical interconnection comprising one or more conductors, wherein each of the plurality of direct independent second electrical interconnections originates at the respective one of the k power subsystem components and terminates at one other of the k power subsystem components without coupling to any other of the k power subsystem components, such that there is no more than a single direct independent electrical interconnection between any two of the k power subsystem components, and , such that the total number of the plurality of direct, independent second electrical interconnections comprises no more than $k*[(k-1)/2]$ direct, independent second electrical interconnections;

wherein each direct independent first electrical interconnection further comprises a connection to a plurality of subsystem regulated buses and a connection to a subsystem unregulated bus; and

wherein each direct independent second electrical interconnection further comprises a connection to at least one of the plurality of subsystem regulated buses and a connection to the subsystem unregulated bus.

Williams fails to teach or suggest each and every limitation of amended claim 33. To assist in the Examiner's understanding of Claim 33, as amended, Applicants refer the Examiner to Figures 2 and 3 of the instant patent application. FIG. 2 shows a high level view of the power architecture of claim 33, with a common power source and k (note that $k=m*n$) power subsystem components. As FIG. 2 clearly shows, and as claim 33 recites, between the common power source component and each of the k subsystems, there is "*a corresponding direct, independent first electrical interconnection that originates at the common power source component and terminates at the respective one of the k power subsystem components without coupling to any other of the k load subsystems*". This also is seen in FIG. 3 of the instant application. In FIG. 3, which is a block diagram of the common power source, the regulated voltage bus 114 of the common power source is electrically connected directly, individually, and independently to each of the $m*n$ (i.e., k) subsystems via direct, individual, independent electrical connection to the

respective regulated buses of these k subsystems. In addition, FIGs. 2 and 3 of the instant application show that between any two of the k power subsystem components there is a “*direct independent second electrical interconnection*” which “*originates at the respective one of the k power subsystem components and terminates at one other of the k power subsystem components without coupling to any other of the k power subsystem components*.”

Williams shows no such direct independent electrical interconnection between his loads 107 or any of his subsystems. Connecting all of the buses 104 of Williams together in a daisy-chain fashion, via switches 109, does not provide a direct independent electrical interconnection between any two loads that does not couple to any of the other loads, as required by claim 33, as amended. The connection is not direct, as required, it is done through other components, and it is not independent, because, at best, the loads 107 are similarly daisy chained together, not connected together directly and independently, as required by claim 33, as amended. This problem with Williams also can be seen in FIG. 3 of Williams, where the load 107 located on the lower left corner of the FIG. 3 is indirectly connected (via the buses 106 and 104) to the load 107 located the bottom middle of FIG. 3 and to the load 107 on the middle right of FIG. 3, but is not directly connected to either load. Thus, Williams does not teach each and every limitation of claim 33, as amended.

For at least the above reasons, the Applicants maintain that claim 33 is patentable over Williams, and the Applicants respectfully requests that the rejection under 35 USC 102 over Williams be withdrawn.

Rejections Under 35 USC 103

The Examiner rejected Claims 1-32 under 35 U.S.C. §103(a) as being unpatentable over Siewert et al. (U.S. Patent number 5,892,299) in view of Hart (U.S. Patent number 6,236,949) and Cole et al. (U.S. Patent number 2,135,250).

Applicants have amended the claims to more precisely claim the invention and to distinguish the present invention over the cited art. In particular, note that Applicants' amendments to claim 1 require [emphasis added]:

a plurality of power source regulated buses, each respective power source regulated bus *originating at a common power source and terminating at a respective one of k load subsystems*, each respective power source regulated bus *directly coupling only the common power source and the respective one of the k load subsystems without coupling to any other of the k load subsystems*;

for each respective one of the k load subsystems, *a plurality of direct independent electrical interconnections between the respective one of the k load subsystems and each other one of the k load subsystems*, each direct independent electrical interconnection comprising one or more conductors, *wherein each direct independent electrical interconnection originates at the respective one of the k load subsystems and terminates at one other of the k load subsystems without coupling to any other of the k load subsystems, such that there is no more than a single direct independent electrical interconnection between any two of the k load subsystems* and such that the total number of the plurality of direct independent electrical interconnections between all of the k load subsystems comprises no more than $k \cdot [(k-1)/2]$ direct, independent electrical interconnections ;

Applicants maintain that Siewert, taken alone or in combination with any (or all) of the art of record, does not teach or suggest either of the above limitations, and further fails to teach or suggest other limitations of claim 1, as amended (as further explained herein). For example, the Examiner suggests that the single bus 1220 of FIG. 12 of Siewert is equivalent to the plurality of power source regulated buses of claim 1, in that the Examiner contends that the text and figures of Siewert allegedly teach a plurality of regulated buses. However, it appears that the Examiner misreads Siewert in a number of ways in applying this reference to claim 1, as amended.

First, note that claim 1 requires not only that there must be a plurality of power source regulated buses, but also that each of these power source regulated buses must originate at a common source (i.e., the same source). This requirement simply is not met anywhere in Siewert, and, in fact, Siewert appears to teach the opposite configuration. For example, in FIGs. 10 and 12 of Siewert (which, per Siewert at col. 11, lines 15-21, have similar operation), although there are shown more than one of a so-called "subgroup common power bus" 1020 (FIG. 10) or 1220 (FIG. 12), each of the subgroup common power buses of Siewert is connected to a different

power source (i.e., one of the 1 to N power source 200 as shown in FIG. 12), not a common power source, as claim 1 requires. Thus, the alleged plurality of power source regulated buses of Siewert do not and cannot “originate at a common power source,” as required by claim 1, as amended.

Second, note that claim 1, as amended further requires that each of the plurality of power source regulated buses that is originating at a common power source further is required to terminate at a respective one of k load subsystems, where, the respective power source regulated bus directly couples ONLY the common power source and the respective one of the k load subsystems without coupling to any other of the k load subsystems. Siewert fails to meet this requirement, as well, for at least several reasons. As a first reason, note that the subgroup common power bus 1220 of FIG. 12 of Siewert does not couple a given load (i.e., protected electrical equipment 1110) directly, but does so through indirectly via isolation device 500. As a second reason, consider FIGs. 10 and 12 of Siewert, which clearly show that the single subgroup common power bus 1220 couples the first power source 200 to a plurality of loads (i.e., protected electrical equipments 1110), not just to a single respective load subsystem without coupling to any other of the load subsystems, as claim 1, as amended clearly requires. **That is, Siewert connects a given power source via a single bus, indirectly, to a plurality of loads. In sharp contrast, the system of claim 1, as amended, connects a given power source directly and independently, via a plurality of regulated power source buses, to a plurality of respective loads (i.e., each load has its own respective power source regulated bus).**

Siewert also fails to teach or suggests “*a plurality of direct independent electrical interconnections between the respective one of the k load subsystems and each other one of the k load subsystems . . . wherein each direct independent electrical interconnection originates at the respective one of the k load subsystems and terminates at one other of the k load subsystems without coupling to any other of the k load subsystems, such that there is no more than a single direct independent electrical interconnection between any two of the k load subsystems*”, as required by claim 1, as amended. Siewert shows absolutely no direct independent electrical interconnections between any protected electrical equipment 1110, where

such an interconnection originates at one subsystem and terminates at another without coupling to any other subsystem, as claim 1 requires. In fact, Siewert shows no direct interconnections whatsoever between protected electrical equipment 1110. At best, Siewert shows that all protected electrical equipment 1110 effectively are connected to each other through the same common power bus - meaning that any given electrical equipment 1110 simultaneously is connected, via the same common power bus, to all other electrical equipment 1110.

Additionally, it appears that Siewert further fails to teach *a power source unregulated bus*, as required by claim 1, as amended. The Examiner contends that the SPSS power bus 1210 of Siewert's FIG. 12 is equivalent to the power source unregulated bus of claim 1. However, Applicants have reviewed Siewert carefully and have failed to find any teaching or suggestion supporting the Examiner's assertion that the SPSS power bus 1210 is unregulated. Siewert is silent as to any express mention as to whether the SPSS power bus 1210 is regulated or unregulated. It can, however, reasonably be deduced from information found in other figures of Siewert that the SPSS power bus 1210 is, in fact, regulated, not unregulated. Consider, for example, Siewert at col. 7, lines 10-15, which describe the power conditioner 400, noting [emphasis added]:

Power Conditioner 400 presents a multiplicity of power conditioner configurations 405, 410, 420, 435, 450, 465, 475 which may be utilized for SPSS operation in any of the embodiments of the present invention shown in FIGS. 1 and 6 to 12. The purpose of a power conditioner is to modify a DC input so as to obtain a desired DC output level. **As an example, a power conditioner may transform 28 VDC unregulated into 5 VDC regulated**, to be utilized in ensuing SPSS operation.

Thus, Applicants maintain that Siewert similarly fails to teach or suggest the power source unregulated bus of claim 1, as amended and, in fact, teaches that the bus that the Examiner is alleging to be unregulated is, in fact, regulated.

Applicants have again carefully reviewed the other references of record (i.e., Hart, Cole, and even Williams), but none of the references of record compensates for Siewert's lack of

teaching (as discussed previously) of the above-described the elements of claim 1, as amended herein.

Thus, for at least the reasons listed above, Applicants maintain that claim 1 is patentable over all of the references of record, taken alone or in combination. Because independent claims 7, 15, and 33 and dependent claims 18 and 19 were amended similarly to the amendments made to claim 1, to add similar limitations as those discussed above in connection with claim 1, Applicants maintain that claims 7, 15, and 33 and dependent claims 18 and 19, together with all claims dependent therefrom, are likewise patentable over the references of record, taken alone or in combination, for at least the same reasons discussed above in connection with claim 1.

As Claims 2 through 6 depend from allowable Claim 1 and cite additional structure, they too are allowable for analogous reasons. As Claims 8 through 14 depend from allowable Claim 7 and cite additional structure, they too are allowable for analogous reasons. In addition, as Claims 16 and 17 and 20 through 32 depend from allowable Claim 15 and cite additional structure, they too are allowable for analogous reasons.

Thus, for at least the reasons given above, Applicants maintain that pending claims 1-33 are allowable over the art of record, taken alone or in combination. Applicants respectfully request that the rejection of these claims be withdrawn. Accordingly, re-examination and reconsideration are requested in view of the above amendment and remarks.

The Examiner is respectfully invited to telephone the undersigning attorney if there are any questions regarding this Response or this application.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0845, including but not limited to, any charges for extensions of time under 37 C.F.R. §1.136.

Respectfully submitted,

Dated: May 28, 2009

DALY, CROWLEY, MOFFORD & DURKEE, LLP

By: /Marianne M. Downing/
Marianne M. Downing
Reg. No. 42,870
Attorney for Applicant(s)
354A Turnpike Street - Suite 301A
Canton, MA 02021-2714
Tel.: (781) 401-9988, Ext. 122
Fax: (781) 401-9966
mmd@dc-m.com

103876

EXHIBIT A

Appl. No.: 10/692,580

Response to Office Action dated December 29, 2008



Standard Mathematical Tables

Fourteenth Edition

EDITOR

SAMUEL M. SELBY, Ph.D.
Distinguished Professor of Mathematics,
Chairman, Mathematics Department
at University of Akron

CONTRIBUTING EDITOR

BRIAN GIRLING, M.S.C.
Northampton College of Advanced Technology
London, England

THE CHEMICAL RUBBER CO.
2310 Superior Avenue, Cleveland, Ohio 44114

© 1964, 1965 by THE CHEMICAL RUBBER CO.

All Rights Reserved

Library of Congress Card No. 30-4052

FACTORIALS

$$n! = e^{-n} n^n \sqrt{2\pi n}, \text{ approximately.}$$

PERMUTATIONS

If $M = {}_n P_r = P_{n,r}$ denotes the number of permutations of n distinct things taken r at a time,—

$$M = n(n-1)(n-2) \cdots (n-r+1) = \frac{n!}{(n-r)!}$$

COMBINATIONS

If $M = {}_n C_r = C_{n,r} = \binom{n}{r}$ denotes the number of combinations of n distinct things taken r at a time,—

$$M = \frac{n(n-1)(n-2) \cdots (n-r+1)}{r!} = \frac{n!}{r!(n-r)!}$$

By definition $\binom{n}{0} = 1$

CUBIC EQUATIONS

A cubic equation, $y^3 + py^2 + qy + r = 0$ may be reduced to the form,—

$$x^3 + ax + b = 0$$

by substituting for y the value, $x - \frac{p}{3}$. Here

$$a = \frac{1}{3}(3q - p^2) \text{ and } b = \frac{1}{27}(2p^3 - 9pq + 27r).$$

For solution let,—

$$A = \sqrt[3]{-\frac{b}{2} + \sqrt{\frac{b^2}{4} + \frac{a^3}{27}}}, \quad B = \sqrt[3]{-\frac{b}{2} - \sqrt{\frac{b^2}{4} + \frac{a^3}{27}}},$$

then the values of x will be given by,

$$x = A + B, \quad -\frac{A+B}{2} + \frac{A-B}{2}\sqrt{-3}, \quad -\frac{A+B}{2} - \frac{A-B}{2}\sqrt{-3}.$$